## REMARKS

Claims 1-40 are pending in this application. Claims 34-36 have been withdrawn from consideration. Claims 37-40 have been rejected. Claims 1-33 have been allowed. Claims 3 and 11 have been amended.

The specification has been objected to because the abstract exceeds 150 words. Applicant has amended the abstract to be less than 150 words. Withdrawal of the objection is respectfully requested.

Claims 37-40 have been rejected under 35 U.S.C. § 102(b) as being anticipated by *Wong* (U.S. Patent No. 6,134,141). This rejection is respectfully traversed.

As understood, *Wong* at best merely discloses a non-volatile memory 200 that includes multiple arrays 130. (Col. 4, lns. 31-35.) A global bias circuit 220 is coupled to a write pipeline 210. The bias global circuit 220 sets a voltage Vvfy on a global line 225 to a voltage level corresponding to a multibit value written in a selected write pipeline 210. (Col. 5, ln. 50-col. 6, ln. 6.) A pullup transistor 242 connects the global line 225 to a row decoder 132 in a selected write pipeline 210 in response to the local control circuit 250. "As a result, global bias circuit 220 charges the selected local row line and connected circuitry including a capacitor 244 to the selected voltage of signal Vvfy. Pullup transistor 242 then shuts off to disconnect the selected row line from the global line 225 and the selected row line remains charged for the write operation and the selected write pipeline 210." (Col. 6, lns. 6-18.) A pulldown transistor 227 grounds the global line 225 in preparation for beginning write operations. (Col. 6, lns. 31-39.)

It is asserted in the Office Action that *Wong* discloses a first bias circuit that generates a bias current Vvfy and includes a current source and first bias transistor 227. Contrary to this assertion, the transistor 227 of *Wong* is a pulldown transistor and is used as a switch for grounding the global line 225 in preparation for beginning write operations. The pulldown transistor 227 does not generate a bias current, and thus is not a first bias circuit as recited in claim 37.

Further, it is asserted in the Office Action that *Wong* discloses a "second bias circuit comprising a plurality of bias current sources (242), each bias current source coupled to the first bias transistor (227) and to a corresponding memory cell and mirroring the bias current . . . ." Contrary to this assertion, the transistor 242 is used as a switch to pass the voltage Vvfy on the global line 225 to the row decoder 132. The transistor 242 is not a bias current source. Further,

the transistor 242 does not mirror a bias current from a first bias circuit as recited in claim 37. Thus, *Wong* does not disclose or even suggest a second bias circuit as recited in claim 37.

Applicant notes that *Wong* does disclose a current mirror 410 that is part of a sense amplifier circuit as shown in Figure 4. The current mirror 410 mirrors current from a reference line. In contrast, claim 37 recites each bias current source of the second bias circuit being coupled to a corresponding memory cell and mirroring the bias current of a first bias circuit. Thus, the current mirror 410 is not the "mirroring" recited in claim 37.

Lacking at least this claim features, *Wong* does not render claim 37 unpatentable. Because claims 38-40 depend on claim 37, for similar reasons *Wong* does not render claims 38-40 unpatentable. Therefore, it is respectfully submitted that claims 37-40 are patentable over the references of record.

The allowance of claims 1-33 is noted. Allowed claims 3, 11, 15 and 18 have been amended merely to correct grammatical errors.

It is submitted that claims 1-33 and 37-40 are allowable, and allowance and issuance of this application is respectfully requested.

Please charge any additional fees, including any fees necessary for extensions of time, or credit overpayment to Deposit Account No. 07-1896, referencing **2102397-991260.**

Respectfully submitted,

**GRAY CARY WARE & FREIDENRICH**

Dated: February 2, 2004 By: Edward B. Weller

Edward B. Weller
Reg. No. 37,468
Attorneys for Applicant(s)

ATTN: Patent Department
GRAY CARY WARE & FREIDENRICH LLP
2000 University Avenue
East Palo Alto, CA 94303-2248
Tel: (650) 833-2000
Fax: (650) 833-2001